GaAs pHEMT MMIC 1.5 WATT POWER AMPLIFIER, 24 - 34 GHz

Typical Applications

The HMC943ALP5DE is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- VSAT
- Military & Space

Features

Saturated Output Power: +33 dBm @ 23% PAE

High Output IP3: +41 dBm

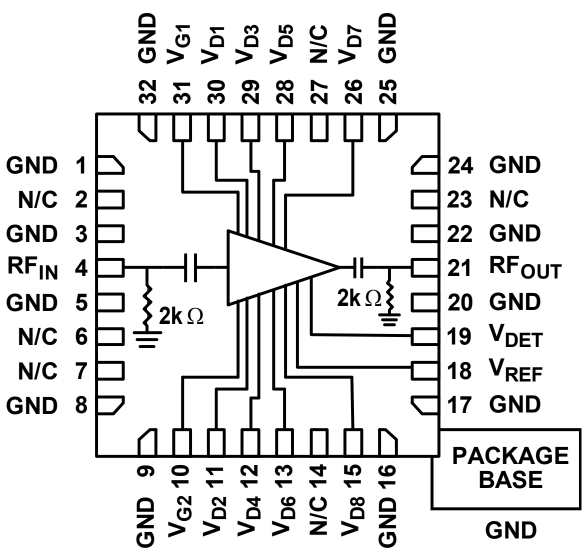
High Gain: 23 dB

DC Supply: +5.5V @ 1300 mA

No External Matching Required

32 Lead 5 x 5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC943ALP5DE is a four stage pHEMT MMIC 1.5 Watt Power Amplifier which operates between 24 and 34 GHz. The HMC943ALP5DE provides 23 dB of gain, and +33 dBm of saturated output power and 23% PAE from a +5.5V supply. The high output IP3 of +41 dBm makes the HMC943ALP5DE ideal for microwave radio applications. A power Detector output is also available The HMC943ALP5DE amplifier I/Os are internally matched to 50 Ohms and is packaged in a leadless QFN 5 x 5 mm surface mount package and requires no external matching components.

Electrical Specifications, T_A = +25° C, Vd1 - Vd8 = +5.5V, Idd = 1300 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		24 - 26.5			26.5 - 31.5			31.5 - 34		GHz
Gain	20	23		19.5	22.5		19.5	22.5		dB
Gain Variation Over Temperature		0.032			0.04			0.044		dB/ °C
Input Return Loss		10			9			8		dB
Output Return Loss		12			10			13		dB
Output Power for 1 dB Compression (P1dB)	29	32		28	31		29	32		dBm
Saturated Output Power (Psat)		33			32			32.5		dBm
Output Third Order Intercept (IP3)[2]		41.5			37			36		dBm
Total Supply Current (Idd)		1300			1300			1300		mA

[1] Adjust V_{G1} or V_{G2} between -2 to 0V to achieve Idd = 1300 mA typical.

[2] Measurement taken at +5.5V @ 1300 mA, Pout / Tone = +22 dBm

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D

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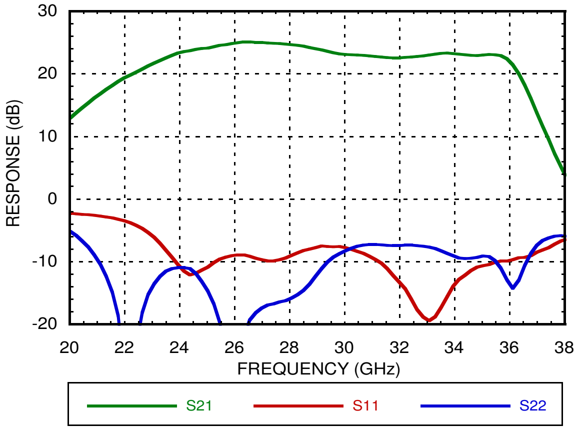
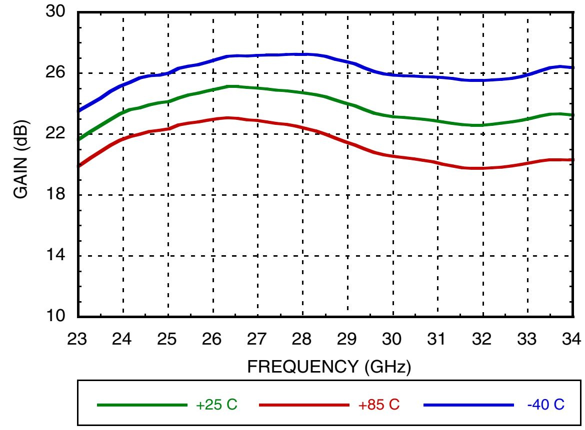
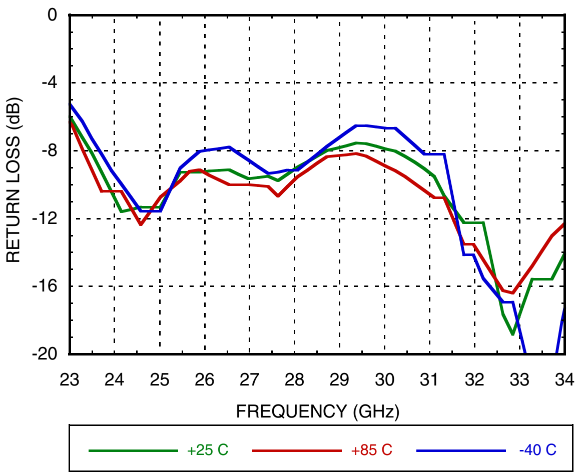
Broadband Gain & Return Loss vs. Frequency



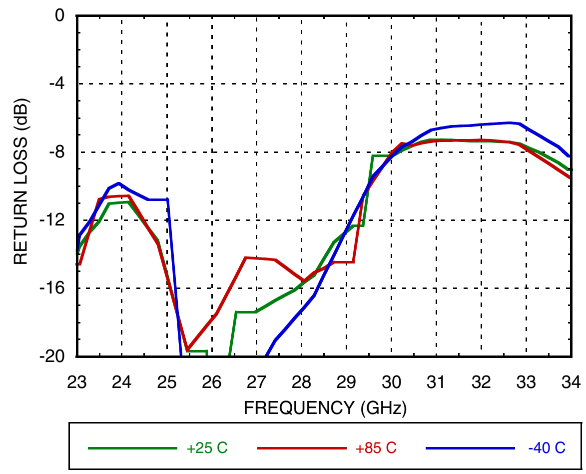
Gain vs. Temperature



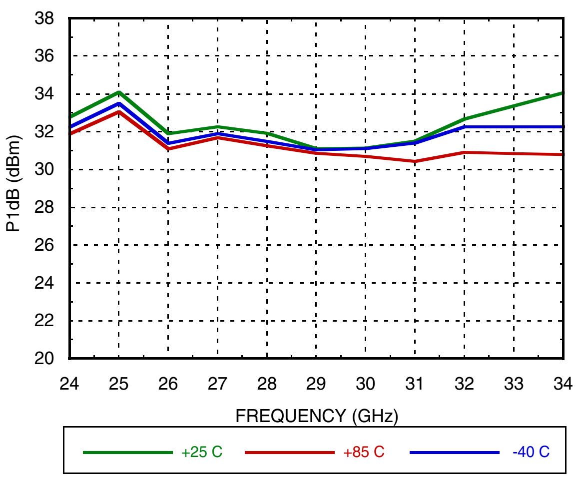
Input Return Loss vs. Temperature



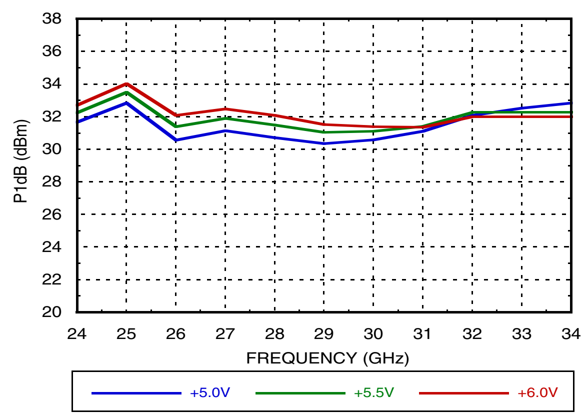
Output Return Loss vs. Temperature



P1dB vs. Temperature



P1dB vs. Supply Voltage (Idd)



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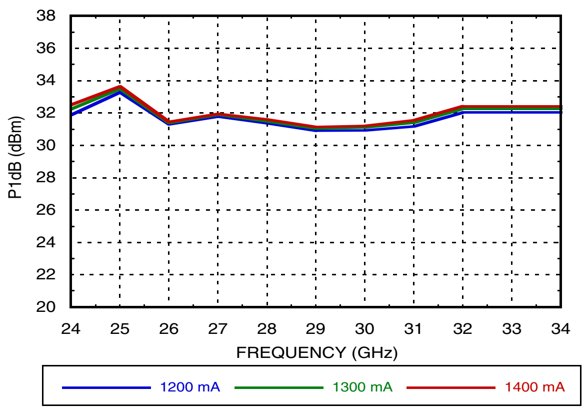
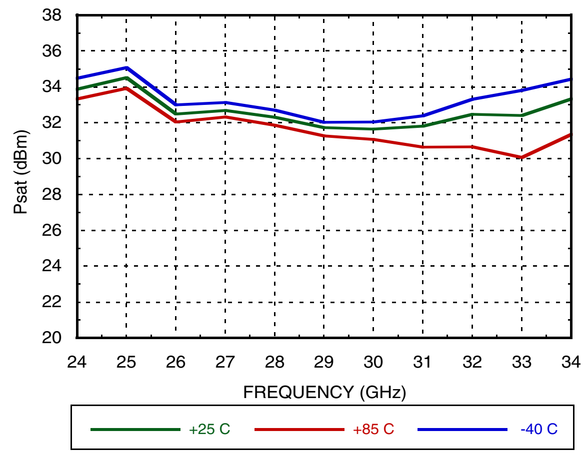
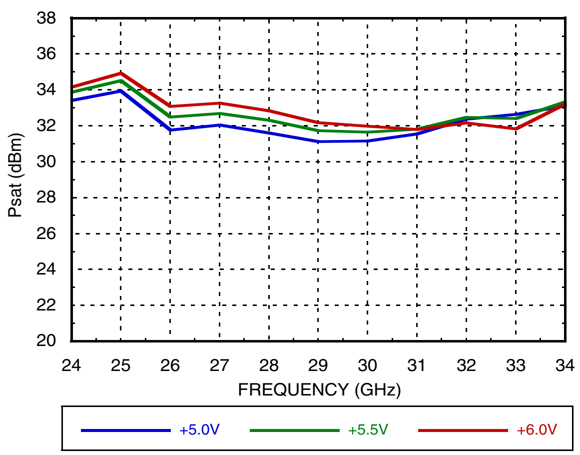
P1dB vs. Supply Current (Idd)



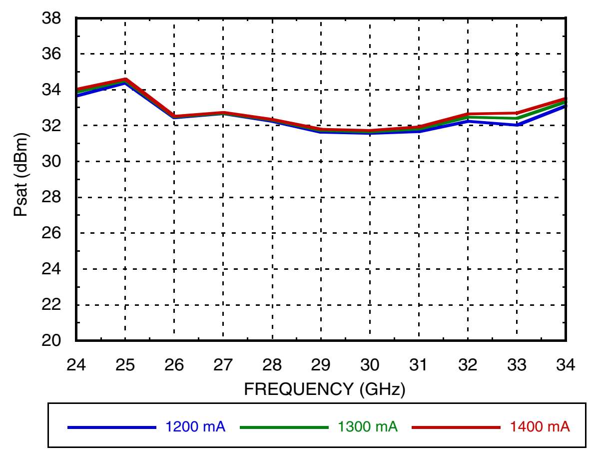
Psat vs. Temparature



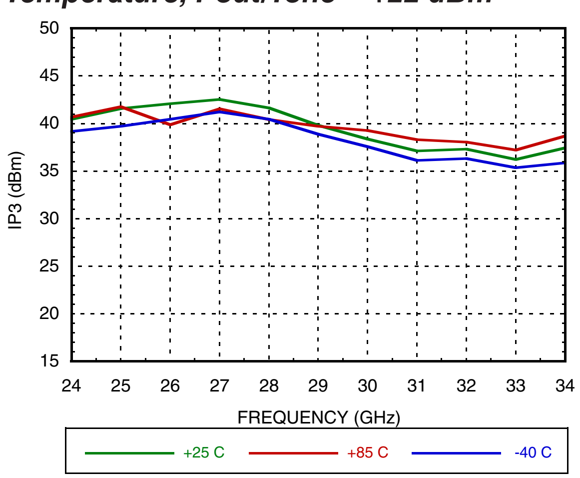
Psat vs. Supply Voltage



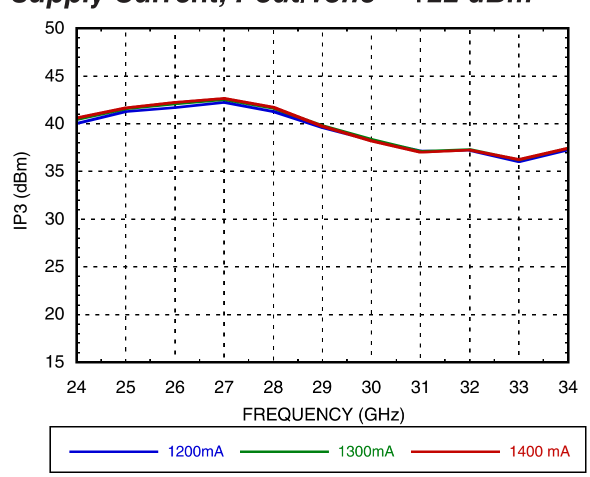
Psat vs. Supply Current



Output IP3 vs. Temperature, Pout/Tone = +22 dBm



Output IP3 vs. Supply Current, Pout/Tone = +22 dBm



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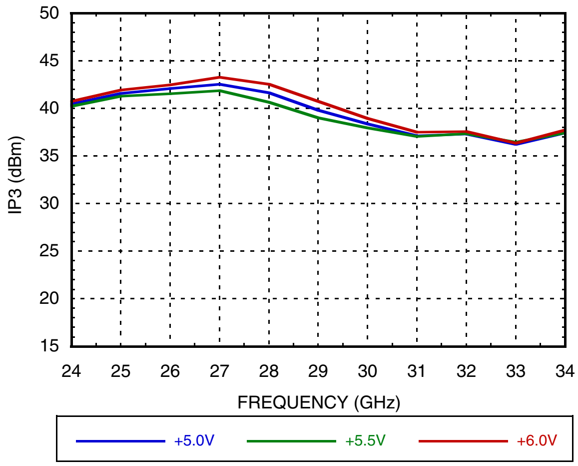
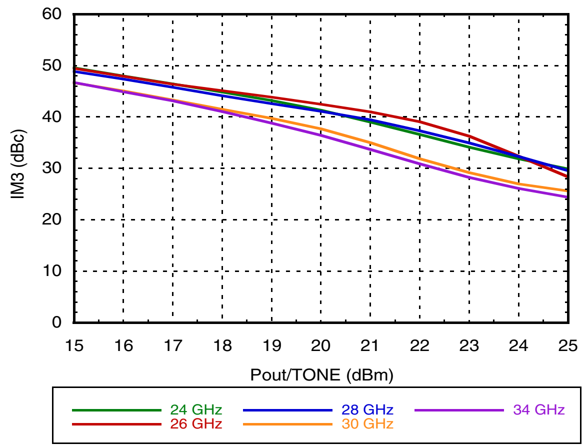
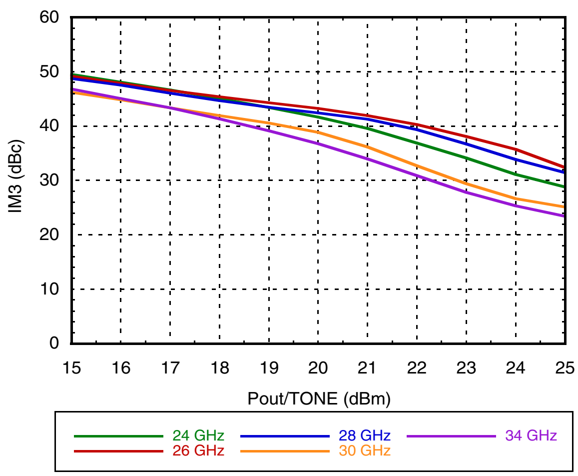
Output IP3 vs. Supply Voltage, Pout/Tone = +22 dBm



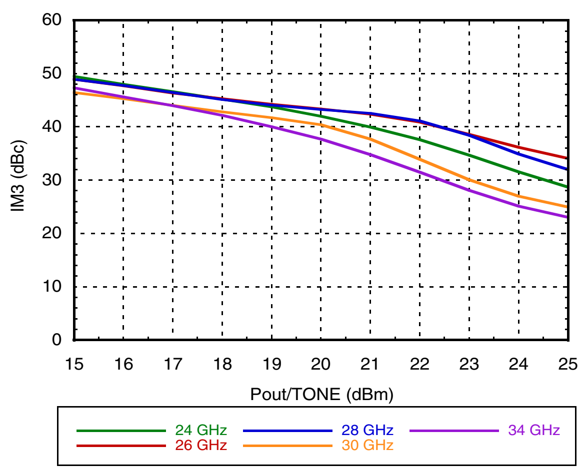
Output IM3 @ Vdd = +5V



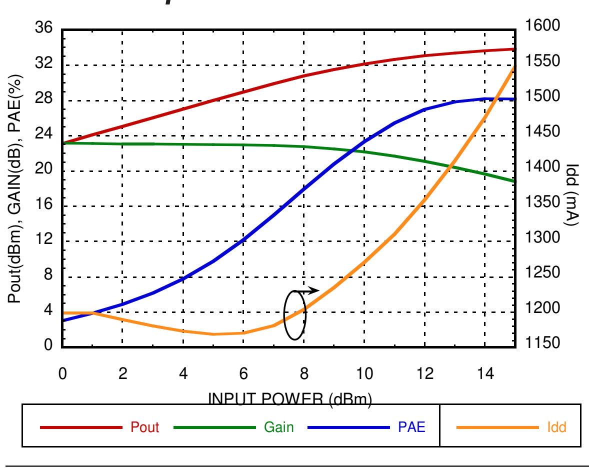
Output IM3 @ Vdd = +5.5V



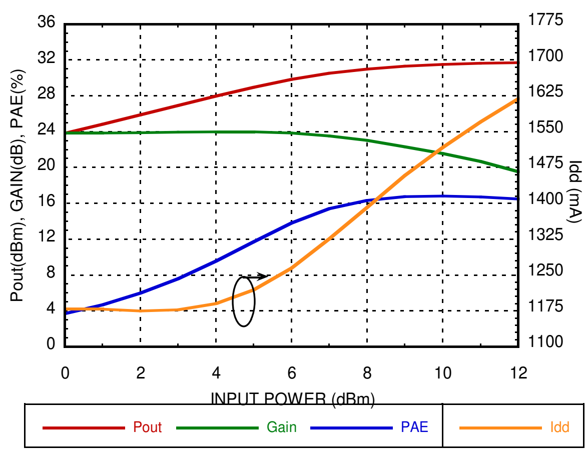
Output IM3 @ Vdd = +6V



Power Compression @ 24 GHz



Power Compression @ 29 GHz



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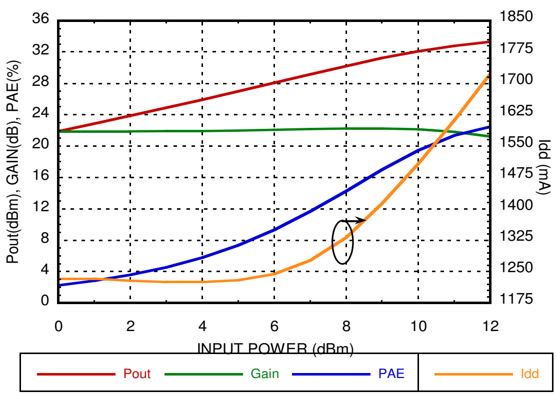
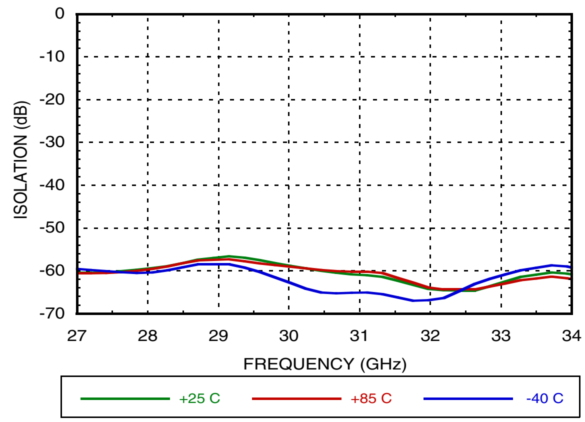
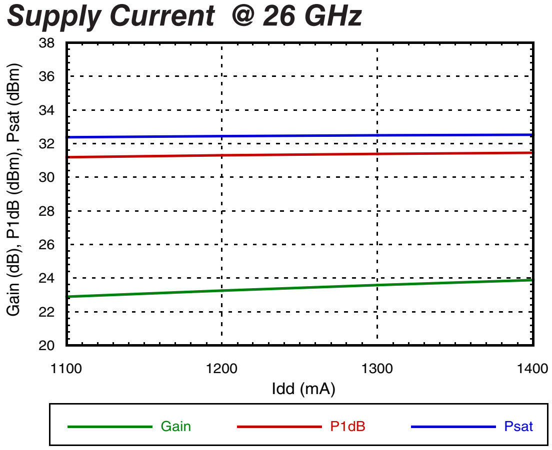
Power Compression @ 34 GHz



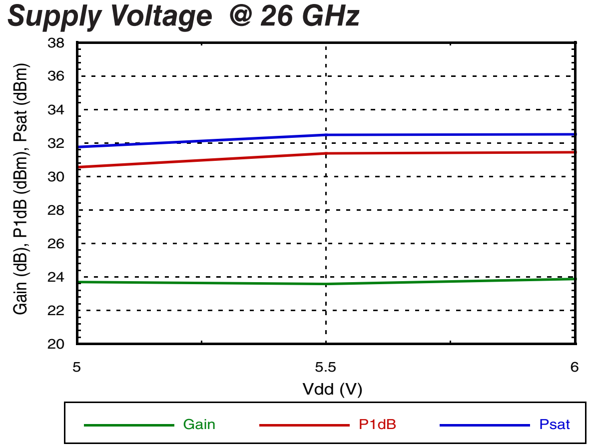
Reverse Isolation



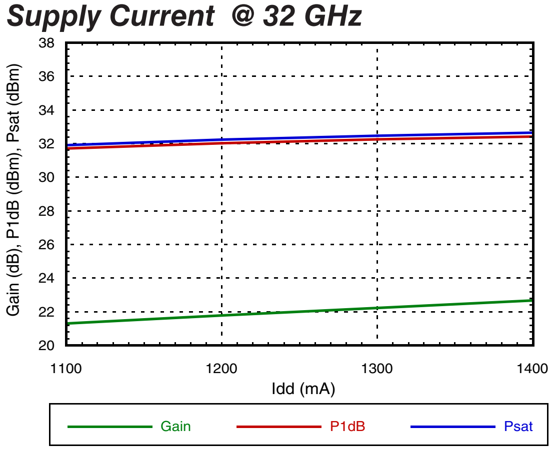
Gain & Power vs. Supply Current @ 26 GHz



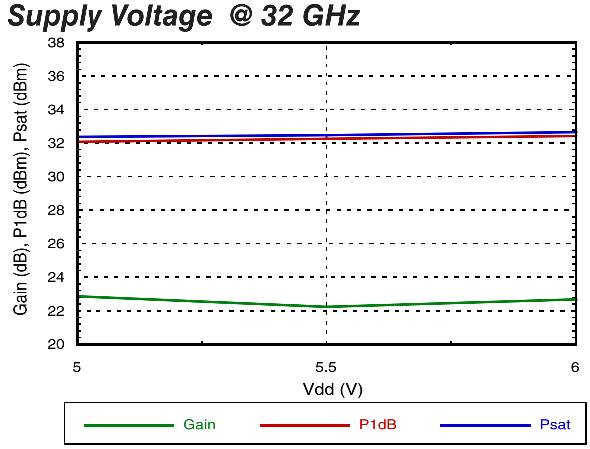
Gain & Power vs. Supply Voltage @ 26 GHz



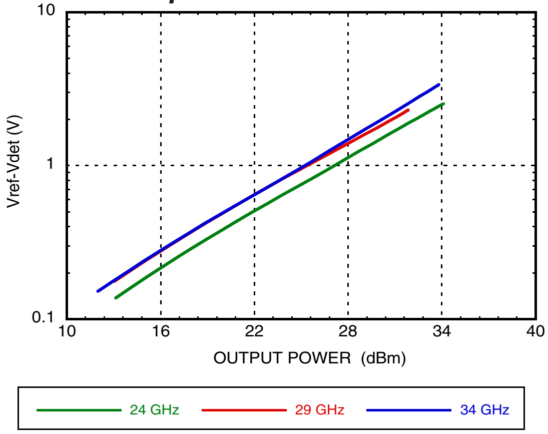
Gain & Power vs. Supply Current @ 32 GHz



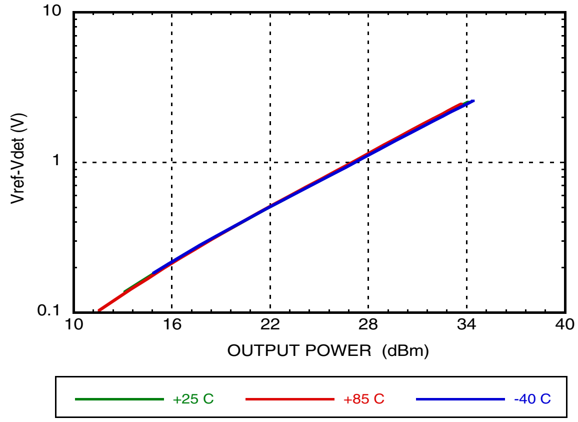
Gain & Power vs. Supply Voltage @ 32 GHz



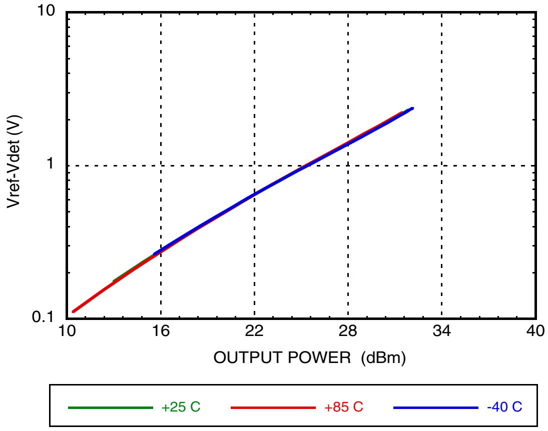
Detector Voltage vs. Output Power at Various Frequencies



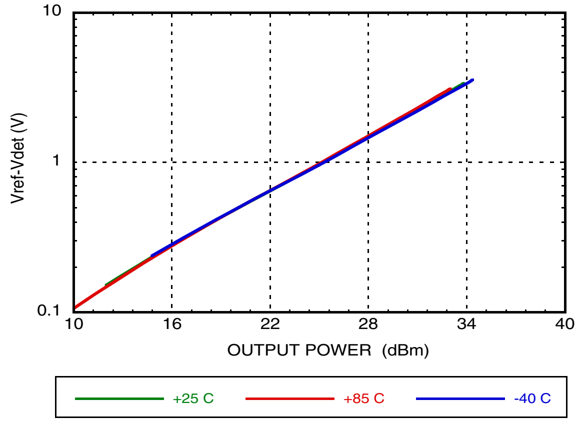
Detector Voltage vs. Output Power at Various Temparatures - 24 GHz



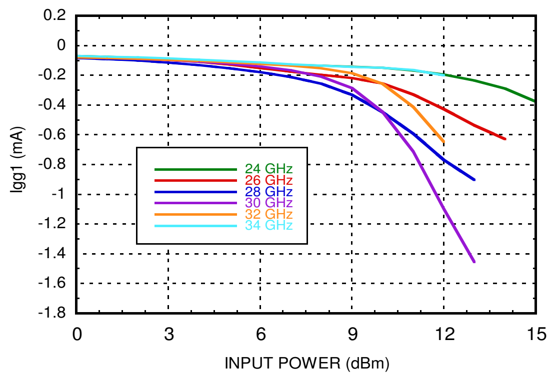
Detector Voltage vs. Output Power at Various Temparatures - 29 GHz



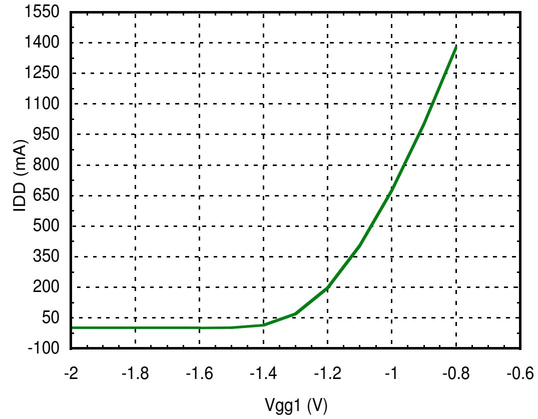
Detector Voltage vs. Output Power at Various Temparatures - 34 GHz



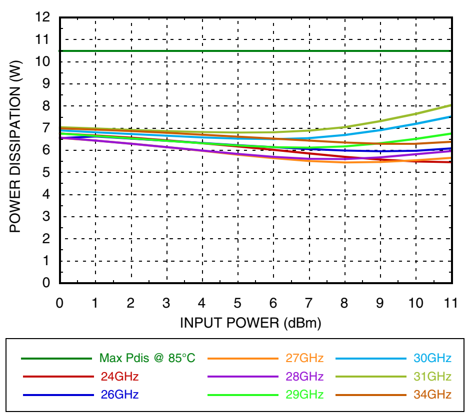
Igg1 vs. Input Power



Idd vs. Vgg1, Representative of a Typical Device



Power Dissipation @ 5.5V, 1300 mA



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Absolute Maximum Ratings

Drain Bias Voltage (Vd)	+6.5V
RF Input Power (RFIN)	+20 dBm
Continuous Pdiss (T= 85 °C) (derate 117 mW/°C above 85 °C)	10.5 W
Storage Temperature	-40 to +125 °C
Max Peak Reflow Temperature	260 °C
ESD Sensitivity (HBM)	Class 0B, 150V

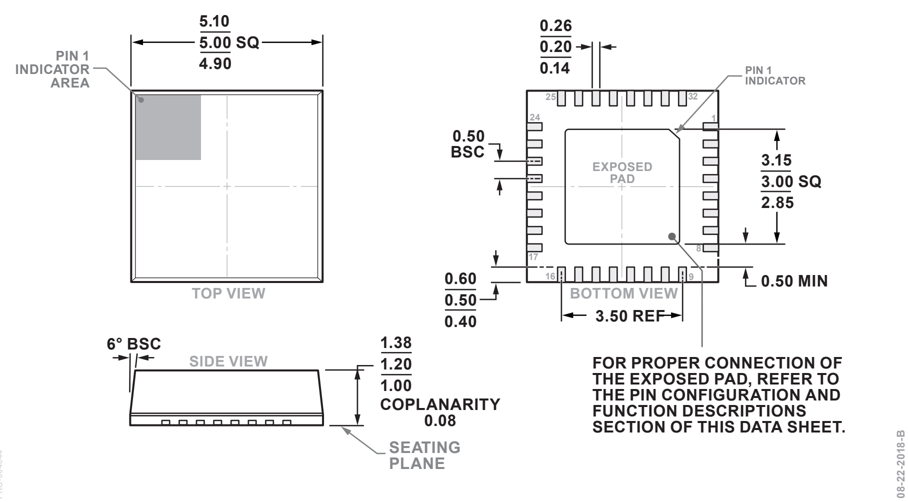
Reliability Information

Junction Temperature to Maintain minimum 1 Million Hour MTTF	175 °C
Nominal Junction Temperature (T=85 °C, Vdd = 5.5 V)	146 °C
Thermal Resistance (channel to ground paddle)	8.6 °C/W
Operating Temperature	-40 to +85 °C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm and 1.20 mm Package Height
(CG-32-1)
Dimensions shown in millimeters.

ORDERING GUIDE

Model	Temperature Range	MSL Rating	Package Description	Package Option	Package Marking [1]
HMC943ALP5DE	−40°C to +85°C	MSL3 [2]	32-Lead LFCSP_CAV	CG-32-1	H943A XXXX

[1] 4 - Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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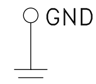
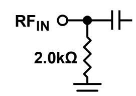
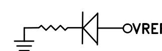
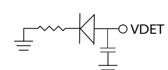
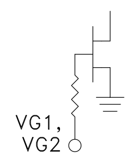
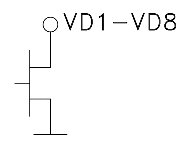
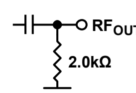
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	These pins and package bottom must be connected to RF/DC ground.	
2, 6, 7, 14, 23, 27	N/C	These pins are not connected internally;however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
4	RFIN	RF signal input. This pad is DC coupled and matched to 50 Ohms over the operating frequency range.	
18	VREF	Reference diode used for temperature compensation of VDET RF output power measurements. Used in combination with VDET, this voltage provides temperature compensation to VDET RF output power measurements. See Figure B for the VREF interface schematic..	
19	VDET	Detector diode used for measurement of the RF output power. Detection via this pin requires the application of a DC bias voltage through an external series resistor. Used in combination with VREF, the difference voltage VREF-VDET is a temperature compensated DC voltage proportional to the RF output power. See Figure A for the VDET interface schematic.	
10, 31	VG1, VG2	Gate control for amplifier. External bypass capacitors of 100 pF, 0.01 µF, and 4.7 µF are required on each. NOTE: VG1 & VG2 are internally connected. So external bias can be applied to either VG1 or VG2	
11 - 13, 15, 26, 28 - 30	VD2, VD4, VD6, VD8, VD7, VD5, VD3, VD1	Drain bias for the amplifier. External bypass capacitors of 100 pF, 0.01 µF, and 4.7 µF are required on each.	
21	RFOUT	RF signal output. This pad is DC coupled and matched to 50 ohms over the operating frequency range.	

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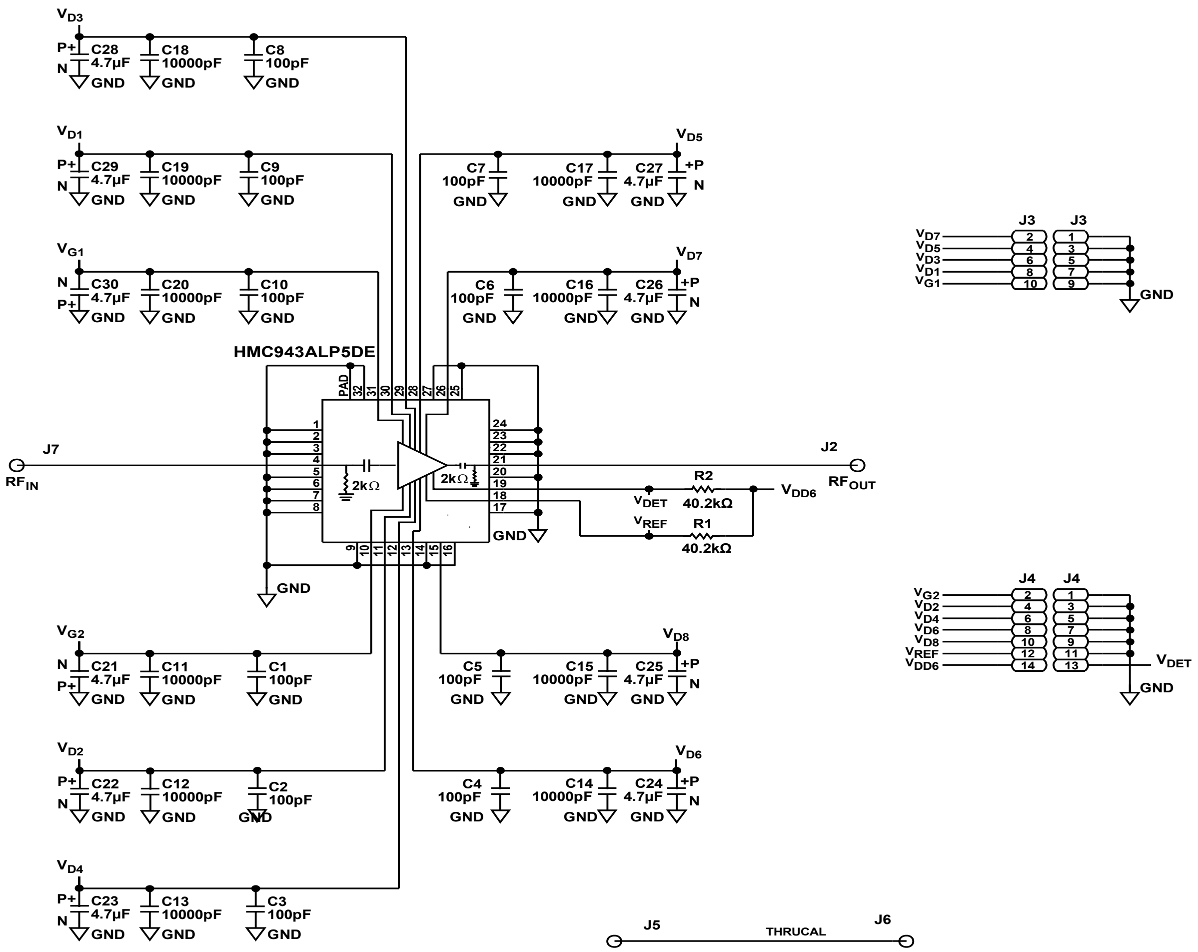
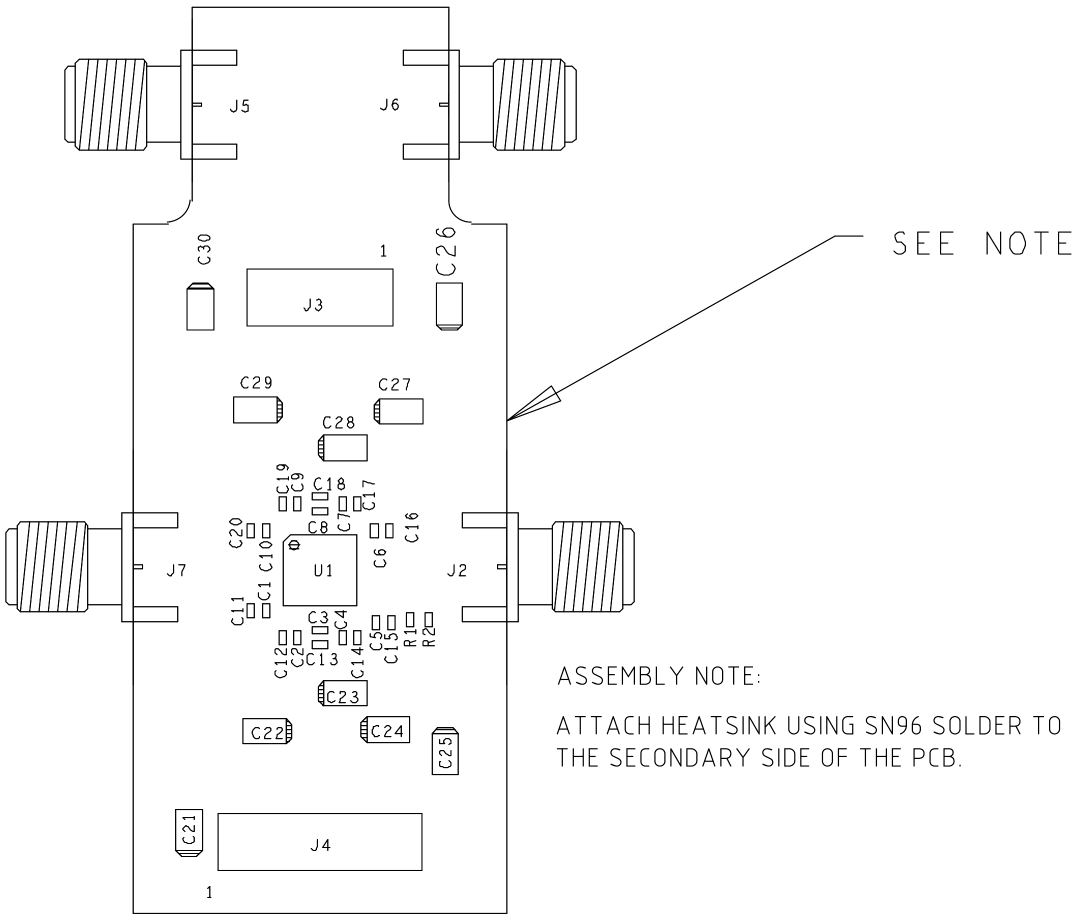
Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB EV1HMC943ALP5D [1]

Item	Description
J7, J2, J5, J6	SRI, K Connectors
J3, J4	DC Pins
C1 - C10	100 pF Capacitors, 0402 Pkg.
C11 - C20	10000 pF Capacitors, 0402 Pkg.
C21 - C30	4.7 µF Capacitors, Case A Pkg.
R1, R2	40.2K Resistors, 0402Pkg
U1	HMC943ALP5DE Power Amplifier
PCB [2]	042915 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices upon request.